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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/706,285 | 11/13/2003 | Richard Greenfield | 1875.3700001 | 5666 |

26111 7590 10/06/2009

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| EXAMINER | |
|---|---|
| ALIA, CURTIS A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2416 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 10/06/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/706,285 | GREENFIELD ET AL. | |
| | Examiner | Art Unit | |
| | Curtis A. Alia | 2416 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-13* is/are rejected.

7)☒ Claim(s) *14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Applicant's amendment filed on 26 May 2009 has been entered. Claims 2, 3, 5-7, 10, 11 and 14-16 have been amended and claims 21-22 have been added. Claims 1-7, 10-16 and 21-22 are still pending in this application, with claims 1, 4 and 7 being independent.

Applicant's request for clarification is explained as follows: Applicant's assumption of the grounds of rejection is correct. Claims 1, 4 and 7 were intended to be placed under the heading of 35 U.S.C. 102(b).

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### *Response to Arguments*

1. Applicant's arguments filed 26 May 2009 have been fully considered but they are not persuasive.

In response to Applicant's argument regarding claims 1, 4 and 7 that Matsumoto does not teach or suggest constraining the number of bits assigned to the bit maps such that a transmission latency does not exceed a predetermined maximum allowed transmission latency, the Examiner disagrees. In particular, Matsumoto does explain reducing the latency by adjusting the assignment of the bits to assign to each bitmap which corresponds to the bit rates at the two different noise phases of the transmission (see column 10, line 54 to column 11, line 23). In the

Examiner's broadest reasonable interpretation of the claims, Matsumoto teaches the claimed limitation. Also, Applicant's interpretation of the claims as recited on page 10 of the Arguments does not read on "achieving an optimum rate versus latency." The claim merely recites minimizing the latency/delay of the transmission, not achieving an optimum rate and latency.

***Double Patenting***

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-2, 4-5, 7 and 10 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8 and 26 of copending Application No. 10/880,769. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

| Instant claims | Copending claims |
|---|---|
| 1. A method for controlling transmission latency in a communications system, wherein the communications system is subject to a noise signal having at least a first noise phase and a second noise phase, the method comprising:<br>determining a first bit rate for symbols transmitted during the first noise phase, and a second bit rate for symbols transmitted during the second noise phase, the first bit rate and the second bit rate being constrained such that a transmission latency does not exceed a predetermined maximum allowed transmission latency; and<br>transmitting symbols at the first bit rate during the first noise phase and at the second bit rate during the second noise phase.<br><br>2. A method accordingly to claim 1, further comprising communicating the predetermined maximum allowed transmission latency via a message to a receiver of the communications system. | 26. A method for controlling transmission latency in a communications system ,wherein the communications system is subject to a time varying noise signal having at least a first noise phase and a second noise phase, the method comprising:<br>communicating a predetermined maximum allowed transmission latency via a message to the constrained rate receiver; and<br>transmitting symbols at the first bit rate during a first noise phase and at a second bit rate during the second noise phase;<br>wherein the first bit rate and the second bit rate are determined by the constrained rate receiver such that a transmission latency is substantially equal to the pre-determined maximum allowed transmission latency.<br><br>36. The method according to claim 8, further comprising maximizing a difference in bit rate between the first bit rate and the second bit rate while maintaining a transmission latency that does not exceed the predetermined transmission latency. |
| 4. An apparatus for controlling transmission latency in a communications system, wherein the communications system is subject to a noise signal having at least a first noise phase and a second noise phase, the apparatus comprising:<br>a constrained rate receiver for determining a first bit rate for symbols transmitted during the first noise phase, and a second bit rate for symbols transmitted during the second noise phase, the first bit rate and the second bit rate being constrained such that a transmission latency does not exceed a predetermined maximum allowed transmission latency; and<br>a constrained rate transmitter for transmitting | 8. A constrained rate transmitter in a communications system that is subject to a time varying noise signal having at least a first noise phase and a second noise phase, the constrained rate transmitter comprising:<br>a latency control transmitter for communicating a pre-determined maximum allowed transmission latency via a message to a constrained rate receiver;<br>wherein the constrained rate transmitter transmits symbols at a first bit rate during the first noise phase and at a second bit rate during the second noise phase;<br>wherein the first bit rate and the second bit rate are determined by the constrained rate receiver |

| | |
|---|---|
| symbols at the first bit rate during the first noise phase and at the second bit rate during the second noise phase.<br><br>5. An apparatus according to claim 4, wherein the constrained rate transmitter further comprising a latency control transmitter for communicating the predetermined maximum allowed transmission latency via a message to the constrained rate receiver. | such that a transmission latency is substantially equal to a pre-determined maximum allowed transmission latency.<br><br>35. The transceiver according to claim 8, wherein the constrained rate receiver is configured to maximize a difference in bit rate between the first bit rate and the second bit rate while maintaining a transmission latency that does not exceed the predetermined transmission latency. |
| 7. A constrained rate receiver for controlling transmission latency in a communications system,<br>wherein the communications system is subject to a noise signal having at least a first noise phase and a second noise phase, the receiver being adapted to determining a first bit rate for symbols transmitted during the first noise phase, and a second bit rate for symbols transmitted during the second noise phase,<br>the first bit rate and second bit rate being constrained such that a transmission latency does not exceed a predetermined maximum allowed transmission latency.<br><br>10. A constrained rate receiver according to claim 7, capable of receiving a message communicating the predetermined maximum allowed transmission latency. | 8. A constrained rate transmitter in a communications system that is subject to a time varying noise signal having at least a first noise phase and a second noise phase, the constrained rate transmitter comprising:<br>a latency control transmitter for communicating a pre-determined maximum allowed transmission latency via a message to a constrained rate receiver;<br>wherein the constrained rate transmitter transmits symbols at a first bit rate during the first noise phase and at a second bit rate during the second noise phase;<br>wherein the first bit rate and the second bit rate are determined by the constrained rate receiver such that a transmission latency does not exceed a pre-determined maximum allowed transmission latency.<br><br>36. The method according to claim 8, further comprising maximizing a difference in bit rate between the first bit rate and the second bit rate while maintaining a transmission latency that does not exceed the predetermined transmission latency. |

Note: while the claims of co-pending application 10/880,769 comprise more limitations than are claimed in the instant application, they do cover each limitation claimed herein.

4. Claims 3, 6 and 11 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 26+36 and 8+35 (respectively) of copending Application No. 10/880,769 in view of Chow (previously cited US 6,009,122).

Regarding claim 3, copending Application No. 10/880,769 does not claim configuring, in accordance with the first bit rate, a first bit allocation table for symbols transmitted during the first noise phase and configuring, in accordance with the second bit rate, a second bit allocation table for symbols transmitted during the second noise phase.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Chow. In particular, Chow teaches configuring, in accordance with a bit rate, a bit allocation table for symbols transmitted during a phase (see column 4, lines 39-54, a superframe bit allocation table is used, wherein a data symbol encoder encodes bits associated with the received data based on the bit allocation table associated with the frame).

In view of the above, having the method of copending Application No. 10/880,769, then given the well-established teaching of Chow, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of copending Application No. 10/880,769 as taught by Chow, since Chow stated in column 4, lines 17-20 that multicarrier modulation systems are able to support multiple bit allocations so that they are able to rapidly alter their bit allocations.

Regarding claim 6, copending Application No. 10/880,769 does not claim a first bit allocation table controller for configuring, in accordance with the first bit rate, a first bit allocation table for symbols transmitted during the first noise phase and a second bit allocation table controller for configuring, in accordance with the second bit rate, a second bit allocation table for symbols transmitted during the second noise phase.

However, the above-mentioned claimed limitation is well known, as evidenced by Chow. In particular, Chow teaches configuring, in accordance with a bit rate, a bit allocation table for symbols transmitted during a phase (see column 4, lines 39-54, a superframe bit allocation table is used, wherein a data symbol encoder encodes bits associated with the received data based on the bit allocation table associated with the frame).

In view of the above, having the apparatus of copending Application No. 10/880,769, then given the well-established teaching of Chow, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the apparatus of copending Application No. 10/880,769 as taught by Chow, since Chow stated in column 4, lines 17-20 that multicarrier modulation systems are able to support multiple bit allocations so that they are able to rapidly alter their bit allocations.

Regarding claim 11, copending Application No. 10/880,769 does not claim a first bit allocation table controller for configuring, in accordance with the first bit rate, a first bit allocation table for symbols transmitted during the first noise phase and a second bit allocation table controller for configuring, in accordance with the second bit rate, a second bit allocation table for symbols transmitted during the second noise phase.

However, the above-mentioned claimed limitation is well known, as evidenced by Chow. In particular, Chow teaches configuring, in accordance with a bit rate, a bit allocation table for symbols transmitted during a phase (see column 4, lines 39-54, a superframe bit allocation table is used, wherein a data symbol encoder encodes bits associated with the received data based on the bit allocation table associated with the frame).

In view of the above, having the method of copending Application No. 10/880,769, then given the well-established teaching of Chow, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of copending Application No. 10/880,769 as taught by Chow, since Chow stated in column 4, lines 17-20 that multicarrier modulation systems are able to support multiple bit allocations so that they are able to rapidly alter their bit allocations.

5. Claims 12-13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8 and 35 of copending Application No. 10/880,769 in view of Amrany et al. (previously cited US 6,580,752).

Regarding claim 12, copending Application No. 10/880,769 does not claim that the first noise phase corresponds to a first signal-to-noise ratio, and the second noise phase corresponds to a second signal-to-noise ratio, the second signal-to-noise ratio being higher than the first signal-to-noise ratio further comprising a second bit rate controller for determining the second bit rate based on the second signal-to-noise ratio.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Amrany. In particular, Amrany teaches that the first noise phase corresponds to a first signal-to-noise ratio (see figure 7, FEXT SRN), and the second noise phase corresponds to a second signal-to-noise ratio (see figure 7, NEXT SNR), the second signal-to-noise ratio being higher than the first signal-to-noise ratio (see column 7, lines 55+, the NEXT noise will be higher than the FEXT noise, thus the FEXT SNR will be higher than the NEXT SNR) further comprising a second bit rate controller for determining the second bit rate based on the second signal-to-noise ratio (see column 8, lines 1-5, since the composite SNR is the lower (usually NEXT) SNR, the bit loading profile is chosen based on the derived SNR of the NEXT phase).

In view of the above, having the receiver of Application No. 10/880,769, then given the well-established teaching of Amrany, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the receiver of Application No. 10/880,769 as taught by Amrany, since Amrany stated in column 2, lines 62-67, the bitrate can be maximized by limiting crosstalk, regardless of network topology.

Regarding claim 13, copending Application No. 10/880,769 does not claim a first bit rate controller for determining the first bit rate based on the second bit rate and the pre-determined maximum allowed transmission latency.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Amrany. In particular, Amrany teaches a first bit rate controller for determining the first bit rate based on the second bit rate and the pre-determined maximum allowed transmission latency

(see column 7, line 39 to column 8, line 6, the bit profile of the FEXT (1st) phase is chosen based on information derived from SNR measured during the NEXT (2nd) phase).

In view of the above, having the receiver of Application No. 10/880,769, then given the well-established teaching of Amrany, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the receiver of Application No. 10/880,769 as taught by Amrany, since Amrany stated in column 2, lines 62-67, the bitrate can be maximized by limiting crosstalk, regardless of network topology.

This is a provisional obviousness-type double patenting rejection.

***Claim Rejections - 35 USC § 102***

6. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated over Matsumoto (previously cited US 6,747,992).

Regarding claim 1, Matsumoto discloses a method for controlling transmission latency in a communications system, wherein the communications system is subject to a noise signal having at least a first noise phase and a second noise phase (see figure 18, noise levels along timeline are varied between NEXT and FEXT noise phases), the method comprising determining a first bit rate for symbols transmitted during the first noise phase, and a second bit rate for symbols transmitted during the second noise phase, the first bit rate and the second bit rate being constrained such that a transmission latency does not exceed a predetermined maximum allowed transmission latency (see column 10, lines 54-60, the bitmaps assigned for each noise phase are

assigned so as to minimize the transmission delay, the maximum transmission delay possible is the worst value present in both bitmaps), and transmitting symbols at the first bit rate during the first noise phase and at the second bit rate during the second noise phase (see figures 9 and 10 and column 15, lines 3+, the first bitrate is used to transmit data in the FEXT noise phase, and the second bitrate is used to transmit data in the NEXT noise phase, these bitrates are different).

Regarding claim 4, Matsumoto discloses an apparatus for controlling transmission latency in a communications system, wherein the communications system is subject to a noise signal having at least a first noise phase and a second noise phase (see figure 18, noise levels along timeline are varied between NEXT and FEXT noise phases), the apparatus comprising a constrained rate receiver for determining a first bit rate for symbols transmitted during the first noise phase, and a second bit rate for symbols transmitted during the second noise phase, the first bit rate and the second bit rate being constrained such that a transmission latency does not exceed a predetermined maximum allowed transmission latency (see column 10, lines 54-60, the bitmaps assigned for each noise phase are assigned so as to minimize the transmission delay, the maximum transmission delay possible is the worst value present in both bitmaps) and a constrained rate transmitter for transmitting symbols at the first bit rate during the first noise phase and at the second bit rate during the second noise phase (see figures 9 and 10 and column 15, lines 3+, the first bitrate is used to transmit data in the FEXT noise phase, and the second bitrate is used to transmit data in the NEXT noise phase, these bitrates are different).

***Claim Rejections - 35 USC § 103***

7. Claims 2-3 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Yong (previously cited US 6,801,570).

Regarding claim 2, Matsumoto does not explicitly teach a latency control transmitter for communicating the predetermined maximum allowed transmission latency via a message to a constrained rate receiver.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Yong. In particular, Yong teaches a latency control transmitter for communicating the predetermined maximum allowed transmission latency via a message to a constrained rate receiver (see column 4, lines 45-54, a rate option generator receives a number of input parameters designating, among other things, a maximum allowed delay for communications between transceivers in the system).

In view of the above, having the method of Matsumoto, then given the well-established teaching of Yong, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of Matsumoto as taught by Yong, since Yong stated in column 3, lines 25-32 that the total number of bits carried by a DMT symbol to different bearer channels are effectively allocated according to channel conditions.

Regarding claim 3, Matsumoto discloses configuring, in accordance with the first bit rate, a first bit allocation table for symbols transmitted during the first noise phase and configuring, in accordance with the second bit rate, a second bit allocation table for symbols transmitted during

the second noise phase (see column 10, lines 31-48, the bit map a is assigned to map the bits for the FEXT noise phase, and the bit map b is assigned to map the bits for the NEXT noise phase).

Regarding claim 5, Matsumoto does not explicitly teach that the constrained rate transmitter further comprises a latency control transmitter for communicating the predetermined maximum allowed transmission latency via a message to the constrained rate receiver.

However, the above-mentioned claimed limitation is well known, as evidenced by Yong. In particular, Yong teaches that the constrained rate transmitter further comprises a latency control transmitter for communicating the predetermined maximum allowed transmission latency via a message to the constrained rate receiver (see column 4, lines 45-54, a rate option generator receives a number of input parameters designating, among other things, a maximum allowed delay for communications between transceivers in the system).

In view of the above, having the apparatus of Matsumoto, then given the well-established teaching of Yong, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the apparatus of Matsumoto as taught by Yong, since Yong stated in column 3, lines 25-32 that the total number of bits carried by a DMT symbol to different bearer channels are effectively allocated according to channel conditions.

Regarding claim 6, Matsumoto discloses that the constrained rate receiver further comprises a first bit allocation table controller for configuring, in accordance with the first bit rate, a first bit allocation table for symbols transmitted during the first noise phase and a second bit allocation table controller for configuring, in accordance with the second bit rate, a second bit

allocation table for symbols transmitted during the second noise phase (see column 10, lines 31-48, the bit map a is assigned to map the bits for the FEXT noise phase, and the bit map b is assigned to map the bits for the NEXT noise phase).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Long et al. (previously cited US 6,804,267) and Okamura (previously cited US 6,658,024).

Regarding claim 7, Matsumoto discloses a constrained rate receiver for controlling transmission latency in a communications system, wherein the communications system is subject to a noise signal having at least a first noise phase and a second noise phase (see figure 18, noise levels along timeline are varied between NEXT and FEXT noise phases), the constrained rate receiver configured to determine a first bit rate for symbols transmitted during the first noise phase, and a second bit rate for symbols transmitted during the second noise phase, the first bit rate and second bit rate being constrained such that a transmission latency does not exceed a predetermined maximum allowed transmission latency (see column 10, lines 54-60, the bitmaps assigned for each noise phase are assigned so as to minimize the transmission delay, the maximum transmission delay possible is the worst value present in both bitmaps), the constrained rate receiver comprising a first bit rate controller for determining the first bit rate based on the second bit rate and the pre-determined maximum allowed transmission latency (see column 10, lines 54-60, the bitmaps assigned for each noise phase are assigned so as to minimize the transmission delay, the maximum transmission delay possible is the worst value present in

both bitmaps, the bitmaps translate the bit distribution for each noise phase, the worst value being in bitmap B (NEXT phase bitmap), so NEXT phase's bitmap B is what constrains the first bitmap A's number of bits, as well as the minimized transmission latency resulting from the bitmaps).

Matsumoto does not explicitly teach that the signal-to-noise ratio associated with the second noise phase is higher than a signal-to-noise ratio associated with the first noise phase.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Long. In particular, Long teaches that the signal-to-noise ratio associated with the second noise phase is higher than a signal-to-noise ratio associated with the first noise phase (see column 3, lines 58-62, NEXT signal-to-noise ratio is sufficiently high for transmitting low bitrate data).

In view of the above, having the transceiver of Matsumoto, then given the well-established teaching of Long, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the transceiver of Matsumoto as taught by Long, since Long stated that full-duplex communication can be optimized during transceiver training.

Matsumoto and Long do not explicitly teach a second bit rate controller for determining the second bit rate based on a signal-to-noise ratio associated with the second noise phase.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Okamura. In particular, Okamura teaches that a second bit rate controller for determining the second bit rate based on a signal-to-noise ratio associated with the second noise phase (see figure 3 and column 2, lines 19-30, the SNR of the NEXT phase is used to determine the number of bits transmitted in the next phase).

In view of the above, having the transceiver of Matsumoto and Long, then given the well-established teaching of Okamura, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the transceiver of Matsumoto and Long as taught by Okamura, since Okamura stated that the delay of fast data can be minimized.

9. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Long and Okamura as applied to claim 7 above, and further in view of Yong.

Regarding claim 10, Matsumoto, Long and Okamura do not explicitly teach that the receiver is further configured to receive a message communicating the predetermined maximum allowed transmission latency.

However, the above-mentioned claimed limitation is well known, as evidenced by Yong. In particular, Yong teaches that the receiver is further configured to receive a message communicating the predetermined maximum allowed transmission latency (see column 4, lines 45-54, a rate option generator receives a number of input parameters designating, among other things, a maximum allowed delay for communications between transceivers in the system).

In view of the above, having the apparatus of Matsumoto, Long and Okamura, then given the well-established teaching of Yong, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the apparatus of Matsumoto, Long and Okamura as taught by Yong, since Yong stated in column 3, lines 25-32 that the total number of

bits carried by a DMT symbol to different bearer channels are effectively allocated according to channel conditions.

Regarding claim 11, Matsumoto discloses a first bit allocation table controller for configuring, in accordance with the first bit rate, a first bit allocation table for symbols transmitted during the first noise phase and a second bit allocation table controller for configuring, in accordance with the second bit rate, a second bit allocation table for symbols transmitted during the second noise phase (see column 10, lines 31-48, the bit map a is assigned to map the bits for the FEXT noise phase, and the bit map b is assigned to map the bits for the NEXT noise phase).

10. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Okamura.

Regarding claims 21 and 22, Matsumoto discloses that the first bit rate is determined based on the second bit rate and the pre-determined maximum allowed transmission latency (see column 10, lines 54-60, the bitmaps assigned for each noise phase are assigned so as to minimize the transmission delay, the maximum transmission delay possible is the worst value present in both bitmaps, the bitmaps translate the bit distribution for each noise phase, the worst value being in bitmap B (NEXT phase bitmap), so NEXT phase's bitmap B is what constrains the first bitmap A's number of bits, as well as the minimized transmission latency resulting from the bitmaps).

Matsumoto does not explicitly teach that the first noise phase corresponds to a first signal-to-noise ratio, and the second noise phase corresponds to a second signal-to-noise ratio, the second signal-to-noise ratio being higher than the first signal-to-noise ratio and the second bit rate is determined based on the second signal-to-noise ratio.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Okamura. In particular, Okamura teaches that the first noise phase corresponds to a first signal-to-noise ratio, and the second noise phase corresponds to a second signal-to-noise ratio, the second signal-to-noise ratio being higher than the first signal-to-noise ratio and the second bit rate is determined based on the second signal-to-noise ratio (see figure 3, NEXT phase has a corresponding SNR and FEXT phase has a corresponding SNR, the bit rates are directly resulting from the SNR of each noise phase) and the second bit rate is determined based on the second signal-to-noise ratio (see figure 3 and column 2, lines 19-30, the SNR of the NEXT phase is used to determine the number of bits transmitted in the next phase).

In view of the above, having the transceiver of Matsumoto, then given the well-established teaching of Okamura, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the transceiver of Matsumoto as taught by Okamura, since Okamura stated that the delay of fast data can be minimized.

### *Allowable Subject Matter*

11. Claims 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis A. Alia whose telephone number is (571) 270-3116. The examiner can normally be reached on Monday through Friday, 9am-6pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2416

/Curtis A Alia/
Examiner, Art Unit 2416
9/17/2009

CAA